Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-5 (canceled)

Claim 6 (currently amended): A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a bonding wire that is mounted ~~through wire-bonding technology and spans~~to span in an overhead manner across the interposing electrically-conductive trace such that the bonding wire is free of interference with the interposing electrically-conductive trace and an unfilled gap is formed between the bonding wire and the interposing electrically-conductive trace, wherein the bonding wire has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

Claim 7 (canceled)

Claim 8 (previously presented): The BGA package of claim 6, wherein the bonding wire is a gold wire.

Claims 9-10 (canceled)

Claim 11 (currently amended): A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a chip resistor that is mounted ~~through SMT technology and spans~~to span in an overhead manner across the interposing electrically-conductive trace such that the chip resistor is free of interference with the interposing electrically-conductive trace and an unfilled gap is formed between the chip resistor and the interposing electrically-conductive trace, wherein the chip resistor has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

Claim 12 (canceled)

Claim 13 (previously presented): The BGA package of claim 11, wherein the chip resistor is a zero-resistance chip resistor.

Claim 14 (new): The BGA package of claim 6, wherein the bonding wire has one end electrically connected by a first trace to the corresponding via, and the other end electrically connected by a second trace to the corresponding bond finger.